REMARKS

Claims 10-17 are pending in the present application. Claim 10 has been amended.

Priority Under 35 U.S.C. 119

Applicants respectfully note the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copy of the priority document in parent application Serial No. 09/460,987.

Claim Rejections-35 U.S.C. 103

Claims 10-17 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Capote et al. reference (U.S. Patent No. 6,297,560) in view of the Riding et al. reference (U.S. Patent No. 6,083,811). This rejection is respectfully traversed for the following reasons.

The method of mounting a semiconductor device on a mounting substrate of claim 10 includes in combination providing the semiconductor device as including a semiconductor element, a sealing resin and a plurality of terminals, the semiconductor element "having a thickness of 200 μm or less, a first surface wherein circuitry is formed, a second surface, and side surfaces positioned between the first and second surfaces, the sealing resin having a thickness equal to or greater than half a thickness of the semiconductor element so that the first surface is sealed by the sealing resin and

the second and side surfaces are not sealed by the sealing resin, each of the plurality of terminals being electrically connected to the circuitry". Applicants respectfully submit that the prior art as relied upon by the Examiner does not make obvious these features.

The Examiner has primarily relied upon the Capote et al. reference as providing the semiconductor device including a semiconductor element, a sealing resin and a plurality of terminals, as featured in claim 10. The Examiner has apparently relied upon Fig. 4 of the Capote et al. reference, which includes encapsulate material 22 formed on chip 10 around discrete solder bumps 14. The Examiner has however acknowledged that the Capote et al. reference does not disclose the thickness of the semiconductor element, and the thickness of the sealing resin in relation to the thickness of the semiconductor element, as featured in claim 10.

In order to overcome these acknowledged deficiencies of the Capote et al. reference, the Examiner has alleged that the Riding et al. reference discloses "providing a semiconductor device 12 as including a semiconductor element 20 and a sealing resin 22 (as disclosed in col. 4, lines 1-29); the semiconductor element having a thickness of 200 μ or less (as disclosed in col. 4, lines 10-12, wherein the dice has a thickness of 4 mils ≈ 102 μ)".

The Examiner has further alleged "Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the semiconductor element of Capote et al. **could have** a thickness of 200 μ or less, and furthermore that since Capote et al. discloses that the thickness of the sealing resin ranges from 52 to

200 μ, that the sealing resin **could have** a thickness equal to or greater than half a thickness of the semiconductor element. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a semiconductor element having any desired thickness as there is no statement denoting the criticality of the semiconductor element thickness" (our emphasis added). Applicants respectfully disagree for the following reasons.

Applicants respectfully submits that dicing film 22 as illustrated in Figs. 4 and 5 of the Riding et al. reference cannot be interpreted as the sealing resin of claim 10. That is, the sealing resin of claim 10 is featured as sealing the first surface of the semiconductor element where the circuitry is formed, whereby a second surface and corresponding side surfaces of the semiconductor element are not sealed.

In contrast, as described in column 4, lines 51-53 of the Riding et al. reference with respect to Fig. 5, a dicing film 22, such as the kind used when making saw cuts, is applied to **back surface 6** of individual dice 20. Applicants respectfully submit that such a dicing film 22 for use when making saw cuts is not a sealing resin as would be understood by one of ordinary skill. Moreover, dicing film 22 of the Capote et al. reference does not cover circuitry, because dicing film 22 is formed on a back surface of the die. Consequently, even if motivation existed to modify the teaching of the Capote et al. reference to further include the use of dicing film 22 of the Riding et al. reference (which motivation Applicants do not admit exists), the combined teaching would still lack the relationship of sealing resin thickness to thickness of the

semiconductor element, as featured in claim 10. Particularly, since dicing film 22 of the Riding et al. reference is not a sealing resin as would be understood by one of ordinary skill, there would be no motivation to modify the Capote et al. teaching to include a sealing resin having a thickness as featured in claim 10, or to have a thickness relative to the thickness of a semiconductor element as featured in claim 10. Applicants therefore respectfully submit that the method of mounting a semiconductor device on a mounting substrate of claim 10 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 10-17 is improper for at least these reasons.

With further regard to this rejection, as noted above, the Examiner has asserted that the semiconductor element of the Capote et al. reference "could have" a thickness of 200 μm or less, and that the sealing resin "could have" a thickness equal to or greater than half a thickness of the semiconductor element.

Applicants respectfully submit that in order to properly combine references, clear and specific motivation for doing so must be established as provided by the relied upon references. The Examiner has however failed to establish such motivation as provided by the relied upon prior art in the paragraph bridging pages 3-4 of the Office Action. In absence of such established motivation, the Examiner's assertion that the semiconductor element of the Capote et al. reference **could have** the features of claim 10, would appear to be based merely upon impermissible hindsight.

The Examiner has further asserted on page 4 of the current Office Action that

there is no statement denoting the criticality of the semiconductor element thickness. However, contrary to the Examiner's assertion, the criticality of the semiconductor element thickness is disclosed on pages 6 and 7 of the present application with respect to Figs. 2A and 2B. Accordingly, Applicants respectfully submit that the method of mounting a semiconductor device on a mounting substrate of claim 10 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 10-17 is improper for at least these additional reasons.

Claim 11 features that providing of the semiconductor device as including a semiconductor element is featured whereby the semiconductor element has a central portion and a peripheral portion surrounding the central portion, the peripheral portion having a step part. The Examiner has very generally alleged that the Capote et al. reference discloses a peripheral portion of a semiconductor element that has a step part. However, the various figures of the Capote et al. reference do not include a semiconductor element having a peripheral step part. Applicants therefore respectfully submit that the rejection of claim 11 is thus improper for at least these additional reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for

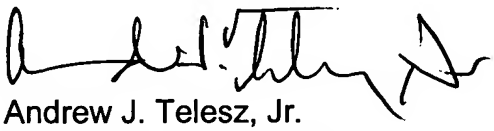
at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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